CML Microcircuits

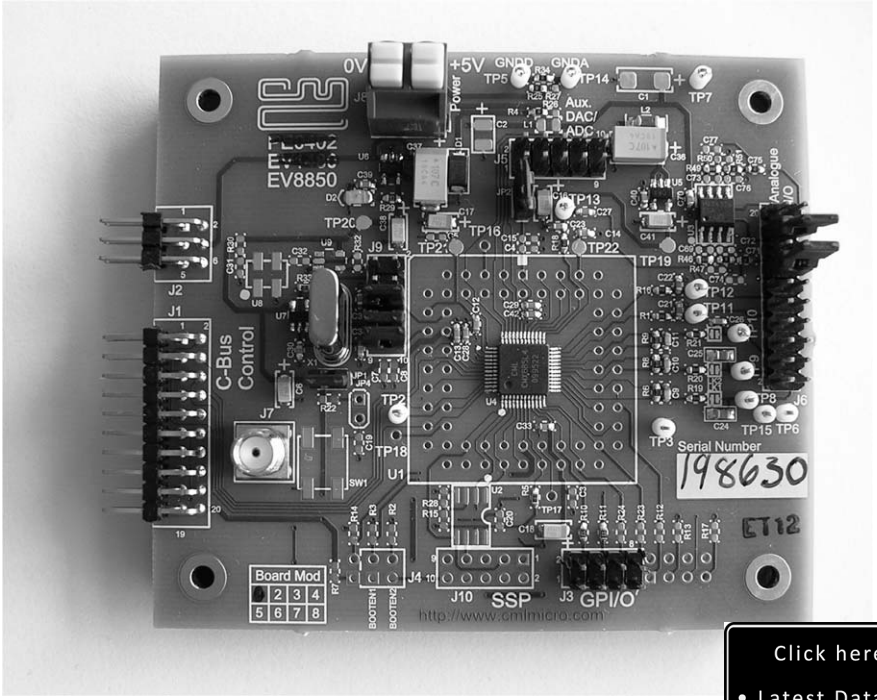
COMMUNICATION SEMICONDUCTORS

EV8850
Evaluation Kit
User Manual

UM8850/1 September 2009

Features

- **CMX885 evaluation**
- **Separate on-board analogue and digital supply regulators**
- **On-board access to all CMX885 signals, commands and data**
- **Command and control by PC via the PE0002 interface card or user's µC development application or emulator**
- **3.6864MHz crystal or external clock input to CMX885**
- **Two on-board uncommitted op amps**



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1 Brief Description

The EV8850 Evaluation Kit is designed to assist in the evaluation and application development of the CMX885 Marine VHF Audio and Signalling Processor. The kit is in the form of a populated PCB comprising a CMX885 IC and appropriate supporting components and circuitry.

The board incorporates all of the necessary power-supply regulation facilities for operation from a single 5 volt supply.

The board is fitted with a C-BUS connector allowing the EV8850 to be operated by connection to either of the two C-BUS ports on a CML PE0002 Interface Card, and used with the associated PC GUI software, or by direct connection between the CMX885 C-BUS and the user's µC development application or emulation system.

CONTENTS

It is always recommended that you check for the latest product datasheet version from the Datasheets page of the CML website: [www.cmlmicro.com].

1.1 History

Version	Changes	Date
2		
1	Original document.	28th Aug '09

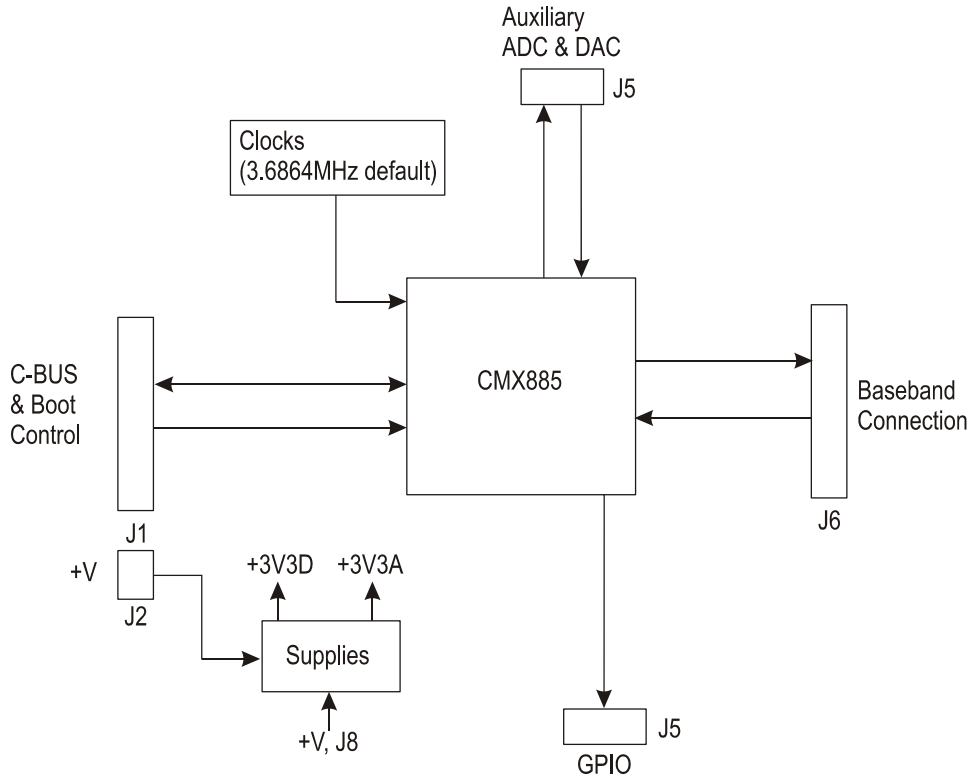

Figure 1 – Block Diagram

2 Preliminary Information

The EV8850 is designed to support the CMX885 Marine VHF Audio and Signalling Processor.

2.1 Laboratory Equipment

The following laboratory equipment is needed to use this evaluation kit:

A 5 Volt dc regulated power supply.

If the EV8850 is being used with the PE0002 Interface Card, the following items will also be required:

1. An IBM compatible PC with the following requirements:
   - One of the following Windows operating systems installed: 2000sp4 or XPsp2.
   - USB port.
   - Minimum screen resolution 800 x 600. Recommended resolution 1024 x 768.
2. A USB type A male to mini B male cable.
3. Software application **ES000221.exe**, or later version, installed on the PC.

2.2 Handling Precautions

Like most evaluation kits, this product is designed for use in office and laboratory environments. The following practices will help ensure its proper operation.

2.2.1 Static Protection

This product uses low power CMOS circuits that can be damaged by electrostatic discharge. Partially damaged circuits can function erroneously, leading to misleading results. Observe ESD precautions at all times when handling this product.

2.2.2 Contents - Unpacking

Please ensure that you have received all of the items on the separate information sheet (EK1480) and notify CML within 7 working days if the delivery is incomplete.

2.3 Approvals

This product is not approved to any EMC or other regulatory standard. Users are advised to observe local statutory requirements, which may apply to this product.

3 Quick Start

This section is divided into two sub-sections. The first is for those users who are using the EV8850 with a PE0002 controller card and its Windows PC GUI software. The second is for users who are using the EV8850 by itself, without a PE0002.

3.1 With PE0002

Note that the C-BUS connector J1 and the power connector J2 are both right angle headers and are designed to plug directly into sockets J5 (C-BUS 1 port) and J9 respectively, or sockets J3 (C-BUS 2 port) and J7 respectively, of a PE0002.

3.1.1 Setting-Up

Refer to the PE0002 user manual and follow the instructions given in the quick start section.

The basic arrangement, when used with the PE0002 is shown below:

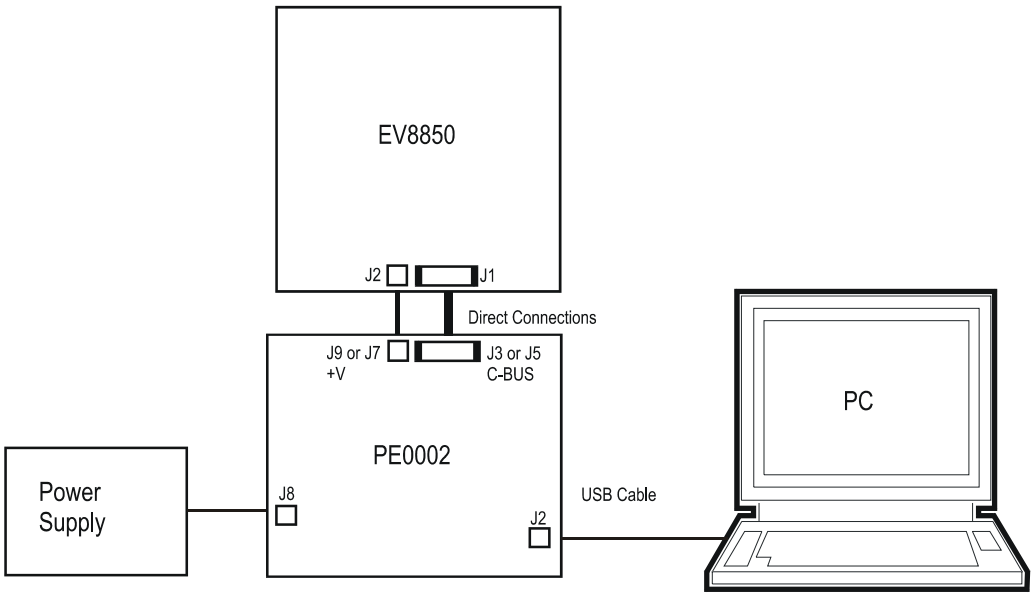

Figure 2 – EV8850 used with PE0002

3.1.2 Operation

The EV8850 should now be ready for evaluation of the CMX885.

3.2 Without PE0002

As an alternative to using the PE0002 controller kit, users may control the CMX885 target device with a user-supplied host controller card. C-BUS connections are made via connector J1.

4 Signal Lists

CONNECTOR PINOUT				
Connector Ref.	**Connector Pin No.**	**Signal Name**	**Signal Type**	**Description**
J1	1, 3, 5, 7, 9, 13 to18	N/C	-	
	2	CSN	I/P	Chip select. Connects to host µC.
	4	CDATA	I/P	Serial Data input. Connects to host µC.
	6	SCLK	I/P	Serial clock input. Connects to host µC.
	8	RDATA	O/P	Serial data output. Connects to host µC.
	10	IRQN	O/P	Interrupt request. Connects to host µC.
	11, 12	GNDD	PWR	Digital supply ground.
	19, 20	+3V3D	PWR	3.3V dc digital supply rail.
J2	1, 2	GNDD	PWR	Digital supply ground.
	3 to 6	+V	PWR	External supply voltage – Daisy chained from PE0002.
J3	1	RXENA	O/P	Receive enabled – active low.
	3	TXENA	O/P	Transmit enabled – active low.
	5, 7	N/C	-	*no connection, do not use.*
	2, 4, 6, 8	GNDD	PWR	Digital supply ground.
J5	1	AUXADC4	I/P	Auxiliary ADC input.
	2	AUXDAC1	O/P	Auxiliary DAC output.
	3	AUXADC3	I/P	Auxiliary ADC input.
	4	AUXDAC2	O/P	Auxiliary DAC output.
	5	AUXADC2	I/P	Auxiliary ADC input.
	6	AUXDAC3	O/P	Auxiliary DAC output.
	7	AUXADC1	I/P	Auxiliary ADC input.
	8	AUXDAC4	O/P	Auxiliary DAC output.
	9, 10	GNDA	PWR	Analogue supply ground.

CONNECTOR PINOUT				
Connector Ref.	**Connector Pin No.**	**Signal Name**	**Signal Type**	**Description**
J6	1	DISCIN	I/P	Discriminator inverting input.
	3	ALTIN	I/P	Alternate inverting input.
	5	MICIN	I/P	Microphone inverting input.
	7	MOD1	O/P	Modulator 1 output.
	9	MOD2	O/P	Modulator 2 output.
	11	AUDIO	O/P	Audio output.
	13	BUF1IN	I/P	High impedance buffered input.
	15	BUF1OUT	O/P	Buffered output.
	17	BUF2IN	I/P	High impedance buffered input.
	19	BUF2OUT	O/P	Buffered output.
	2, 4, 6, 8, 10, 12, 14, 16, 18, 20	GNDA	PWR	Analogue supply ground.
J7		CLKEXT	I/P	External input option for CMX885 clock.
J8		+V	PWR	External supply voltage.
		0V	PWR	External supply ground.

Table 1 – Signal List

TEST POINTS		
Test Point Ref.	**Default Measurement**	**Description**
TP2	0V	Loop – CMX885 system clock 2 output.
TP3	0V	Loop – CMX885 system clock 1 output.
TP5	0V	Loop – GNDD, digital ground.
TP6	0V	Loop – GNDA, analogue ground.
TP7	0V	Loop – GNDA, analogue ground.
TP8	-	Loop – DISCIN - Discriminator inverting input.
TP9	-	Loop – ALTIN - Alternate inverting input.
TP10	-	Loop – MICIN - Microphone inverting input.
TP11	HiZ	Loop – MOD1 - Modulator 1 output.
TP12	HiZ	Loop – MOD2 - Modulator 2 output.
TP13	HiZ	Loop – AUDIO - Audio output.
TP14	0V	Loop – GNDA, analogue ground.
TP15	0V	Loop – GNDA, analogue ground.
TP19	3.3V	Pad – Output from on-board regulator. DC supply voltage for analogue rail.
TP20	3.3V	Pad – Output from on-board regulator. DC supply voltage for digital rail.
TP21	2.5V	Pad – CMX885 internally generated voltage.
TP22	0V	Pad – CMX885 VBIAS.

Table 2 – Test Points

JUMPERS			
Link Ref.	**Positions**	**Default Position**	**Description**
JP1	1-2	Short	Isolates digital supply rail from CMX885.
JP2	1-2	Short	Isolates analogue supply rail from CMX885.
J9	1-2	Open	*no connection, do not use.*
	3-4	Open	External clock source.
	5-6	Short	Crystal clock source – if components fitted by customer.
	7-8	Short	Ground external clock input.
	9-10	Short	Crystal clock source – if components fitted by customer.
J6	13-14	Short	Ground input to uncommitted buffer1.
	17-18	Short	Ground input to uncommitted buffer2.

Table 3 – Jumpers

LEDs	
LED Ref.	**Description**
D2	Indicates that the digital supply voltage is present.

Table 4 – LEDs

Notes:

BI	=	Bidirectional
HiZ	=	High impedance
I/P	=	Input
N/C	=	Not connected
O/P	=	Output
PWR	=	Power supply connection

5 Circuit Schematics and Board Layouts

For clarity, circuit schematics are available as separate high-resolution files. These can be obtained via the CML website.

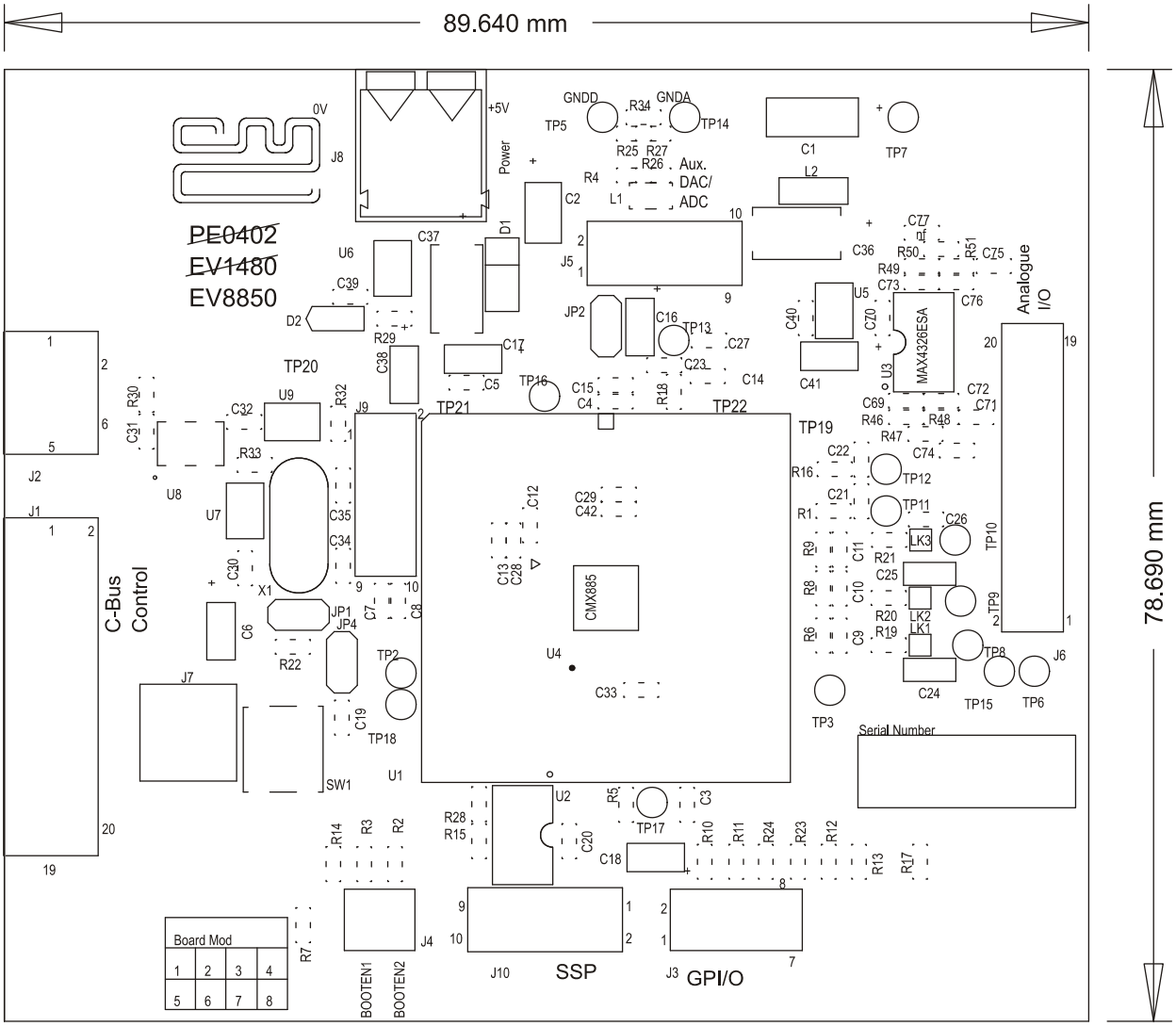

Figure 3 – PCB Layout: Top

6 Detailed Description

6.1 Hardware Description

6.1.1 Power Supplies

The board is fitted with two voltage regulators: U5 and U6 provide the analogue and digital supply rails respectively. The input to these two regulators should be provided by an external 5V dc regulated power supply, which can be daisy chained from the PE0002 or connected to the board via connector J8, a push type connector.

The analogue and digital supply voltage levels can be monitored on test points TP19 and TP20 respectively.

LED illumination confirms the on-board presence of the +3.3V dc digital voltage supply.

6.1.2 Clock Options

The PCB is designed to provide two CMX885 device clock options. The board is supplied with a 3.6864MHz quartz crystal oscillator circuit (C34, C35 and X1).

Header J9 is used with jumper sockets to select the required option as shown in the table below. Shaded cells illustrate locations where a jumper socket should be fitted.

J4 Jumper Position	**Clock Option**	
	External	Quartz crystal (default)
1-2		
3-4		
5-6		
7-8		
9-10		

Table 5 – Clock Select Jumper Positions

6.1.3 Control Interface

The CMX885 C-BUS is brought out on connector J1. This is a right angle male header designed to plug directly into the PE0002 interface card that has a matching female header.

6.1.4 Baseband Interfacing

Connector J5 provides access to Auxiliary ADCs 1 to 4 and Auxiliary DACs 1 to 4 of the CMX885 device.

The CMX885 baseband input amplifiers for DISC, ALT and MIC are configured as ac coupled, unity gain, inverting amplifiers. The inputs to these circuits are fed from connector J6.

The CMX885 baseband outputs, MOD1, MOD2 and AUDIO, are fed through an RC network to connector J6.

A dual op amp IC is fitted to the board, with both amplifiers configured as unity-gain buffers. It is possible to set up other op amp based configurations with the addition of passive components to the PCB footprints provided. It is recommended that 0603 sized surface mount components be used. Access to the input and output of each of these uncommitted amplifiers is also from connector J6.

6.1.5 Digital Interfacing

Connector J3 provides access to the receive and transmit enable outputs of the CMX885, RXENA and TXENA respectively.

6.2 Adjustments and Controls

None.

6.3 Software Description

When used with a PE0002, the 'Function Image Load' and 'Program Serial Memory' tabs are not relevant to the EV8850.

There is a range of PE0002 scripts available from the CML website demonstrating a range of CMX885 features.

6.4 Evaluation Tests

The following examples can be used to verify control of the CMX885 via the C-BUS interface. These registers can be programmed using the 'C-BUS Control' tab in the PE0002 software.

6.4.1 Write to and Read from a Register

- Write any 16-bit number to register $C0.
  The data transferred to the device on the Command Data pin looks like this:
  { C0 } { <ms byte> } { <ls byte> } ..... Command Data

- The value written to this register (the Powerdown Control register) can be read back from register $C4 by issuing a single command byte, then reading two data bytes from the Reply Data pin, as follows:
  { C4 } ..... Command Data
  { <ms byte> } { <ls byte> } ..... Reply Data

Note that the power consumption of the device will increase once this register has been written to, since some parts of the device will no longer be powersaved.

6.4.2 Check Transmit Voice Path

Configure the CMX885 with the C-BUS register data given in Table 6.

	C-BUS Register	
Write Data	Address	Name
$5F40	$C0	Powerdown Control
$7700	$B0	Analogue Gain
$02B0	$B1	Input Gain and Signal Routing
$3000	$A7	AuxADC and Tx MOD Mode
$1400	$C2	Audio Control
$4002	$C1	Mode Control

Table 6 – CMX885 Register Settings – Transmit Voice Path

Apply a 1kHz, audio signal to MICIN (J6 pin 5 or TP10), at a level of -10dBm (the maximum signal level before distortion is about +1dBm).

Check the audio signal at the MOD1 output pin (J6 pin 7 or TP11). The level should be nominally +/- 1dB of the input signal.

6.4.3 Check Receive Voice Path

Configure the CMX885 with the C-BUS register data given in Table 7.

Write Data	C-BUS Register	
	Address	Name
$38C0	$C0	Powerdown Control
$000E	$B0	Analogue Gain
$0050	$B1	Input Gain and Signal Routing
$1400	$C2	Audio Control
$4001	$C1	Mode Control

Table 7 – CMX885 Register Settings - Receive Voice Path

Apply a differential 1kHz, audio signal to DISCIN (J6, pin 1 or TP8) at a level of 0dBm.

Check the audio signal coming out of the CMX885 AUDIO output pin (TP13).
The level should be –3.2dBm (+/- 1dB).

6.4.4 Generate Two External Digital Clocks

Configure the CMX885 with the C-BUS register data given in Table 8.

Write Data	C-BUS Register	
	Address	Name
$0000	$C0	Powerdown Control
$1D27	$AB	System Clock 1 PLL Configuration
$E026	$AC	System Clock 1 Reference and Source Configuration
$1BF3	$AD	System Clock 2 PLL Configuration
$E626	$AE	System Clock 2 Reference and Source Configuration

Table 8 – CMX885 Register Settings - External Digital Clocks

With the default 3.6864MHz clock input, a digital clock frequency of 4.088MHz should be observed at the system clock 1 output (TP3) and a frequency of 16.346MHz should be observed at the system clock 2 output (TP2).

Now write 0xC026 to either $AC or $AE registers to turn off the System Clock 1 or System Clock 2 outputs, respectively.

7 Performance Specification

7.1 Electrical Performance

7.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the Evaluation Kit.

	Min.	Max.	Units
Supply (+V – 0V)	-0.3	9.0	V
Voltage on any connector pin to V_{SS}	-0.3	3.6	V
Current into or out of +V and V_{SS} pins	0	+0.45	A
Current into or out of any other connector pin	-20	+20	mA

7.1.2 Operating Limits

Correct operation of the Evaluation Kit outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply (+V – 0V)		4.5	5.5	V
External Clock Frequency		3.0	24.576	MHz

7.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

Evaluation Device Clock Frequency = 3.6864MHz, +V = 5.0V, Tamb = +25°C.

For CMX885 parameters, see CMX885 data sheet.

	Notes	Min.	Typ.	Max.	Units
DC Parameters					
I_{DD}	1, 2	-	6	9	mA
+3V3A		3.15	3.3	3.45	V
+3V3D		3.15	3.3	3.45	V
Analogue Parameters					
Output Impedances					
Mod1, Mod2 and Audio	3	-	100	-	kΩ
Buf1out and Buf2out	4	-	0.1	-	Ω
Input Impedances					
IP1, IP2 and IP3		-	50	-	kΩ
Buf1in and Buf2in	4	1	-	-	MΩ
External Clock Input					
'High' pulse width		21	-	-	ns
'Low' pulse width		21	-	-	ns
Input impedance		10	-	-	MΩ

Notes:
1. Total PCB current consumption, CMX885 in idle mode.
2. Not including any current drawn from pins by external circuitry.
3. Small signal impedance.
4. When configured, as supplied, as unity gain buffers.

7.1.4 Operating Characteristics - Timing Diagrams

Please refer to the CMX885 Datasheet for details.

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